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09/800,039

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EXAMINER

PRENTY, MARK V

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 11/08/2002

6

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.
09/800,039

Applicant(s)
SAGARWALA et al.

Examiner
Prenty

Art Unit
2822



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Sep 3, 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 and 27-39 is/are pending in the application.
- 4a) Of the above, claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 and 27-39 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____ 6) ☐ Other:

This Office Action is in response to the amendment filed September 3, 2002.

Claims 1-7 and 28-39 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Independent claim 1 is indefinite because "a minimum channel length required for the p-channel transistors" and "a minimum channel length for the respective p-channel transistor," are indefinite.

Claims 2-7 depend on independent claim 1 and are thus similarly indefinite.

Dependent claim 5 is further indefinite because "a distance below which the transistor will not operate reliably due to short channel effects," and "a distance above which the transistor will not turn on efficiently," are indefinite.

Dependent claim 6 is further indefinite because "a distance below which the transistor will not operate reliably due to short channel effects," and "a distance above which the transistor will not turn on efficiently," are indefinite.

Independent claim 28 is indefinite because "a minimum channel length required for the p-channel transistor" is indefinite.

Claims 29-32 depend on claim 28 and are thus similarly indefinite.

Claim 29 is further indefinite because "the minimum channel length required for the p-channel transistor" is indefinite.

Claims 30-32 depend on claim 29 and are thus similarly indefinite.

Claim 30 is further indefinite because "the minimum channel length required for the p-channel transistor" and "a diffusion distance for implanted dopants forming source and drain regions for the p-channel transistor," are indefinite.

Claim 32 is further indefinite because "a minimum channel length required for

the n-channel transistor” is indefinite.

Independent claim 33 is indefinite because “a minimum channel length required for the p-channel transistor” is indefinite.

Claims 34-39 depend on independent claim 33 and are thus similarly indefinite.

Claim 35 is further indefinite because “the minimum channel length required for the p-channel transistor” and “a diffusion distance for implanted dopants forming source and drain regions for the p-channel transistor,” are indefinite.

Claims 36 and 37 depend on claim 35 and are thus similarly indefinite.

Claim 27 is rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, has possession of the claimed invention. Specifically, claim 27 has been amended to recite “first and second sidewall spacers,” but the specification describes only a first sidewall spacer (see Fig. 11’s element 38).¹

Claims 33 and 34, at least insofar as understood, are rejected under 35 U.S.C. §102(b) as being anticipated by Miyajima et al. (United States Patent 5,273,914 submitted in the Information Disclosure Statement filed May 24, 2001).

With respect to independent claim 33, Miyajima et al. disclose an intermediate structure for use in forming a CMOS integrated circuit (see Fig. 13(g)), comprising: a p-type region 2 for an n-channel transistor including lightly doped source and drain regions 8; an n-type region 3 for a p-channel transistor without lightly doped source and drain regions; a gate electrode 6 overlying a portion of the n-type region, the gate

¹ Amended claim 27’s “first and second sidewall spacers” refers to first and second distinct sidewall spacers formed on the same side of the gate electrode (both of which are formed on both sides of the gate electrode), not to the same first sidewall spacer formed on both sides of the gate electrode. See claim 27 as originally filed. See also the applicant’s remark concerning Chen at the first full paragraph on page 14 of the response.

electrode having a width less than "a minimum channel length required for the p-channel transistor"; and at least one conformal insulating layer 22 over a top and sides of the gate electrode 6, the insulating layer having a thickness which, taken on opposing sides of the gate electrode and combined with the width of the gate electrode, exceeds "a minimum channel length required for the p-channel transistor."

Claim 33, at least insofar as understood, is thus rejected under 35 U.S.C. §102(b) as being anticipated by Miyajima et al.

With respect to dependent claim 34, Miyajima et al's insulating layer 22 forms a mask for implanting source and drain regions for the p-channel transistor.

Claim 34, at least insofar as understood, is thus rejected under 35 U.S.C. §102(b) as being anticipated by Miyajima et al.

Claim 27, at least insofar as understood, is rejected under 35 U.S.C. §102(e) as being anticipated by Chen (United States Patent 5,766,991 submitted in the Information Disclosure Statement filed May 24, 2001).

With respect to independent claim 27, Chen discloses a CMOS integrated circuit structure (see Fig. 13), comprising: an n-channel transistor including lightly doped source and drain regions within a p-type region 10 of a substrate 14; and a p-channel transistor without lightly doped source and drain regions within an n-type region 12 of the substrate, the p-channel transistor including: a gate electrode having a width less than a channel length of a channel for the p-channel transistor; and first sidewall spacers adjacent opposing sides of the gate electrode and overlying a portion of the channel for the p-channel transistor and portions of source and drain regions 74 and 75 for the p-channel transistor.

Claim 27, at least insofar as understood, is thus rejected under 35 U.S.C.

§102(e) as being anticipated by Chen.

Claims 28-30 and 32, at least insofar as understood, are rejected under 35 U.S.C. §102(e) as being anticipated by Chen (United States Patent 5,766,991 submitted in the Information Disclosure Statement filed May 24, 2001).

With respect to independent claim 28, Chen discloses a CMOS integrated circuit structure (see Fig. 13), comprising: an n-channel transistor including lightly doped source and drain regions within a p-type region 10 of a substrate 14; and a p-channel transistor without lightly doped source and drain regions within an n-type region 12 of the substrate, the p-channel transistor including: a gate electrode having a width less than a channel length of a channel for the p-channel transistor; and first sidewall spacers adjacent opposing sides of the gate electrode and overlying at least a portion of the channel for the p-channel transistor and portions of source and drain regions 74 and 75 for the p-channel transistor, wherein the width of the gate electrode is less than "a minimum channel length required for the p-channel transistor."

Claim 28, at least insofar as understood, is thus rejected under 35 U.S.C. §102(e) as being anticipated by Chen.

With respect to dependent claim 29, Chen's first sidewall spacers have a width which, taken on opposing sides of the gate electrode and combined with the width of the gate electrode, exceeds "the minimum channel length required for the p-channel transistor."

Claim 29, at least insofar as understood, is thus rejected under 35 U.S.C. §102(e) as being anticipated by Chen.

With respect to dependent claim 30, Chen's first sidewall spacers have a width which, taken on opposing sides of the gate electrode and combined with the width of

the gate electrode, exceeds “the minimum channel length required for the p-channel transistor” plus “a diffusion distance for implanted dopants forming source and drain regions for the p-channel transistors.”

Claim 30, at least insofar as understood, is thus rejected under 35 U.S.C. §102(e) as being anticipated by Chen.

With respect to dependent claim 32, Chen’s n-channel transistor further comprises: a gate electrode having a width approximately equal to a “minimum channel length required for the n-channel transistor”; and sidewall spacers adjacent to opposing sides of the n-channel transistor gate electrode and overlying the lightly doped source and drain regions.

Claim 32, at least insofar as understood, is thus rejected under 35 U.S.C. §102(e) as being anticipated by Chen.

The applicant’s argument with respect to the maintained rejection of claims 1-7 and 28-39 under 35 U.S.C. §112, second paragraph, is not persuasive. Specifically, the applicant’s argument “the Office Action does not explain how those limitations are indefinite,” is not persuasive.

With respect to independent claim 1, its “a minimum channel length required for the p-channel transistors” and “a minimum channel length for the respective p-channel transistor” limitations are indefinite on their face.

With respect to dependent claim 5, its “a distance below which the transistor will not operate reliably due to short channel effects” and “a distance above which the transistor will not turn on efficiently” limitations are indefinite on their face.

With respect to dependent claim 6, its “a distance below which the transistor will not operate reliably due to short channel effects” and “a distance above which the

transistor will not turn on efficiently” limitations are indefinite on their face.

With respect to independent claim 28, its “a minimum channel length required for the p-channel transistor” limitation is indefinite on its face.

With respect to dependent claim 29, its “the minimum channel length required for the p-channel transistor” limitation is indefinite on its face.

With respect to dependent claim 30, its “the minimum channel length required for the p-channel transistor” and “a diffusion distance for implanted dopants forming source and drain regions for the p-channel transistor” limitations are indefinite on their face.

With respect to dependent claim 32, its “a minimum channel length required for the n-channel transistor” limitation is indefinite on its face.

With respect to independent claim 33, its “a minimum channel length required for the p-channel transistor” limitation is indefinite on its face.

With respect to dependent claim 35, its “the minimum channel length required for the p-channel transistor” and “a diffusion distance for implanted dopants forming source and drain regions for the p-channel transistor” limitations are indefinite on their face.

The applicant’s argument with respect to the rejection of claims 33 and 34 under 35 U.S.C. §102(b) as being anticipated by Miyajima et al. is not persuasive. Specifically, the applicant cites independent claim 33’s indefinite “a minimum channel length required for the p-channel transistor” limitation. However, as explained above, Miyajima et al. anticipates indefinite claims 33 and 34, at least insofar as understood.

The applicant’s argument with respect to the rejection of claim 27 under 35 U.S.C. §102(e) as being anticipated by Chen is not persuasive. Specifically, the

applicant's argument "Independent claim 27 recites that first and second sidewalls ... Such a feature is not shown or suggested by the cited references ... Chen teaches removing the (second) silicon nitride sidewalls 76 through 79..." (emphasis in original), is misplaced, because the applicant discloses only first sidewall spacers (see Fig. 11's element 38, for example), not first and second sidewall spacers (see the rejection of claim 27 under 35 U.S.C. §112, first paragraph, above). In any event, Chen's Fig. 13 sidewall spacer, like this application's Fig. 11 sidewall spacer 38, overlies a portion of the channel for the p-channel transistor and portions of source and drain regions for the p-channel transistor.

The applicant's argument with respect to the rejection of claims 28-30 and 32 under 35 U.S.C. §102(e) as being anticipated by Chen is not persuasive. Specifically, the applicant cites independent claim 28's indefinite "a minimum channel length required for the p-channel transistor" limitation. However, as explained above, Chen anticipates indefinite 28-30 and 32, at least insofar as understood.

Applicants' amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL.** See M.P.E.P. §706.07(a). Applicants are reminded of the extension of time policy set forth in 37 C.F.R. §1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. §1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

Registered practitioners can telephone the examiner at (703) 308-4939. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the application's Serial Number. Technology Center 2800's general telephone number is (703) 308-0956.

Mark Prenty
Mark V. Prenty
Primary Examiner